REMARKS

The present response is filed with a Request for Continued Examination (RCE) and is to the Office Action mailed in the above-referenced case on December 12, 2003, made Final. Claims 1-14 are pending in the application. Claims 1-14 stand rejected under 35 U.S.C. 102(e) as being anticipated by Chow et al. (U.S. 5,999,528), hereinafter Chow. Applicant has again carefully studied the reference of Chow cited and applied by the Examiner, and the Examiner's statements in the instant Office Action. In response, applicant provides further argument that not all of the limitations of applicant's claims are explicitly taught in the prior art reference, and the reference therefore still fails as a primary reference in the Examiner's prima facie rejection of applicant's claims.

In the previous response filed by applicant responding to the Office Action dated August 13, 2003, applicant argued extensively that Chow clearly teaches a single switching plane, not a plurality of switching planes, as is specifically taught in applicant's invention, and recited in applicant's claims. The Examiner has kindly responded to applicant's previous argument in the Response to Argument section of the instant Office Action, stating that Chow discloses in Fig. 15, a switching core 1 made up of a plurality of dual switching cards such as 1A, 1B, etc., providing inter-shelf links for connecting peripheral shelves (col. 6, lines 46-50). The Examiner adds that the switching fabric can be fully duplicated (col. 6, lines 64 - 65) and that the modifications and duplication to the switching core 1 is possible for redundancy and to enhance possible distribution of system timing signals col. 24, lines 13-22.

Applicant has very carefully reviewed the cited and applied portions of Chow referenced above, as well as the remainder of the reference, and applicant strongly argues that nowhere in the cited portions is there any explicit teaching of

applicant's claimed plurality of switching planes, and the Examiner has taken the teachings of Chow out of context in applying the teachings as anticipating all of the limitations of applicant's claims.

Specifically, applicant argues that even though the single switching plane of Chow contains multiple line cards, it remains that Chow teaches only a single switching plane, not a plurality of switching planes as in applicant's invention. Applicant's invention incorporates multiple switching planes, each of which includes multiple switching channels, each of which are assignable to transfer data associated with one data port of one of the interface units. As a further limitation in applicant's broadest claim, if the number of interface units is less than the number of switching channels in any one of the plurality of switch planes, then reallocation of the switching resources is performed such that multiple channels of at least one switch plane can be assigned to transfer data of multiple ports of at least one of the interface units, resulting in switch plane channels being used to transfer the data, which would otherwise be unused. Such reallocation of switch plane channels is thereby possible, resulting in the illumination of one or more switch planes from the switch fabric, which results in substantially reduced hardware complexity and cost.

Furthermore, and most importantly, applicant argues that not all of the limitations have been addressed by the Examiner in any of the Office Actions to date, which is required for supporting a valid prima facie rejection. For convenience, applicant reproduces claim 1 in its present form below.

Claim 1 recites:

1. A method of reallocating switching circuitry in a switching fabric to permit data transfer among a plurality of interface units each having a plurality of data

ports, the switching fabric being partitionable into a plurality of switch planes such that each switch plane is assignable to transfer data associated with a data port of the plurality of interface units and each switch plane including multiple switching data communication links each being assignable to transfer data associated with one data port of one of the interface units, the method comprising:

determining a number of interface units connected to the switching fabric;

determining a number of switching data communication links in each switch plane ; and

if the number of interface units is less than the number of switching data communication links in each switch plane, for at least one of the plurality of switch planes, assigning a first data communication link in the switch plane to transfer data associated with a first data port of a first interface unit and assigning a second data communication link in the switch plane to transfer data associated with a second data port of the first interface unit.

Applicant wishes to focus the Examiner's attention on the specific functional limitation recited : "if the number of interface units is less than the number of switching data communication links in each switch plane, for at least one of the plurality of switch planes, assigning a first data communication link in the switch plane to transfer data associated with a first data port of a first interface unit and assigning a second data communication link in the switch plane to transfer data associated with a second data port of the first interface unit." Applicant regards the above specific limitation to be a significant limitation in the claim, and a key and patentable aspect, which the Examiner has so far, not specifically addressed in <u>any</u> of the Office Actions to date. Upon carefully and

thorough review of the reference of Chow, applicant is very confident that there is no specific teaching anywhere in the reference of the above limitation.

Applicant asserts that for a valid prima facie rejection, each and every limitation of applicant's claims must be addressed by the Examiner, and the specific portion(s) of the reference relied upon by the Examiner supporting the rejection and disclosing each limitation must be shown to applicant, and it must also be explained by the Examiner how the teaching in the specific portion(s) reads on the claimed limitation.

Applicant therefore asserts that, since the Examiner has only dealt with the architecture of applicant's invention, and has only cited and applied portions of the reference of Chow which teach architecture, and the above very important functional limitation of applicant's claims has, to date, not been addressed by the Examiner, a prima facie rejection is not made, and Chow fails to anticipate applicant's base claims. Simply showing how the architecture of the prior art reference reads on applicant's claimed architecture clearly cannot anticipate the functional limitations of the method claim.

Therefore, even if applicant were to accept the Examiner's contention that Chow anticipates the architecture of applicant's claimed invention, i.e. a plurality of switching planes, which applicant maintains that the reference clearly does not, Chow could not possibly teach the above key and patentable limitation of assigning a first data communication link in the switch plane to transfer data associated with a first data port of a first interface unit and assigning a second data communication link in the switch plane to transfer data associated with a second data port of the first interface unit, if the number of interface units is less than the number of switching data communication links in each switch plane, for at least one of the plurality of switch planes.

In view of applicant's above arguments presented that Chow fails to teach

applicant's architecture, as well as fails to teach all of the specific limitations of applicant's base claims, applicant believes it has been clearly and unarguably demonstrated that applicant's method claim 1 is therefore patentable over the reference of Chow for the reasons stated above. Applicant's independent claim 8 is the apparatus claim in accordance with method claim 1, and recites the same specific limitations as argued above by applicant on behalf of claim 1. The Examiner has rejected claim 8 using the same rationale as applied to the rejection of claim 1. Claim 8, therefore, is also clearly and unarguably patentable over the reference of Chow as argued above. Depending claims 2-7 and 9-14 are then patentable on their own merits, or at least as depended from a patentable claim.

As all of the claims standing for examination, as argued above by applicant, have been shown to be clearly and unarguably patentable over the rejection of the Examiner, applicant respectfully requests reconsideration and that the present case be passed quickly to issue. If there are any time extensions due beyond any extension requested and paid with this amendment, such extensions are hereby requested. If there are any fees due beyond any fees paid with the present amendment, such fees are authorized to be deducted from deposit account 50-0534.

Respectfully Submitted,

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by _____

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